Room-Temperature Quantum Confinement Effects in Transport Properties of Ultrathin Si Nanowire Field-Effect Transistors

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Supporting Information

ABSTRACT: Quantum confinement of carriers has a substantial impact on the physics of nanoscale device operation. We present electrical transport analysis for lithographically fabricated sub-5 nm thick Si nanowire field-effect transistors and show that confinement-induced quantum oscillations prevail at 300 K. Our results discern the basis of recent observations of performance enhancement in ultrathin Si nanowire field-effect transistors and provide direct experimental evidence for theoretical predictions of enhanced carrier mobility in strongly confined nanowire devices.

KEYWORDS: Quantum confinement effects, Si nanowires, room-temperature quantum oscillations, top-down patterning, ultrathin Si nanowire transistor

Quantum confinement of carriers has an extensive influence on the physics of nanoscale device operation. However, experimental study of quantum confinement effects was mostly limited to ultralow temperatures until recent years due to relatively large channel diameters of devices. For practical applications of quantum characteristics, it is crucial for such effects to manifest at room temperature, which naturally dictates the size of the channel be reduced well into single-digit nanometer range so that the quantum size effect is able to overcome thermal broadening. In recent years, quantum oscillatory behavior has been reported to persist at elevated temperatures in one-dimensional (1D) devices with reduced dimensions. There has been considerable effort to improve key device parameters such as transfer conductance and carrier mobility of such narrow Si nanowire (SiNW) devices. More recently, it has been possible to lithographically (top-down) fabricated SiNW FETs on silicon-on-insulator (SOI) substrates with device diameters as small as 3 nm, and significant performance enhancement has been reported at 300 K in top-down patterned sub-5 nm p-Si [110] NW FETs. Here, we demonstrate quantum confinement effect in transport properties of ultrathin p-Si FETs at room temperature. Clear plateau-like structures in drain–source current ($I_{DS}$) are revealed in the subthreshold region of sub-5 nm p-SiNW FETs at 300 K. Oscillations in both transconductance ($g_M$) and channel conductance ($g_D$) are analyzed with respect to quantum confinement-induced subband structure. The genuine oscillatory behaviors of conductance and carrier mobility are understood in terms of strong confinement of carriers in quantized 1D subband structure with corresponding unique 1D density of states (DOS). We compile the findings of our study into a framework to present clear experimental evidence of measurable quantum confinement effects (at 300 K) and also justify the recently reported enhanced carrier mobility in sub-5 nm SiNW FETs at room temperature.
Method. To demonstrate quantum size effects at room temperature, we fabricated sub-5 nm thick Si[110] NW FETs lithographically on a SOI substrate, and performed high-resolution transmission electron microscopy (HR-TEM) imaging to confirm dimensions and uniformity of channel bodies in measured devices. Figure 1 shows a three-dimensional (3D) schematics of the device and HR-TEM images of the cross section of a nanowire body before (a) and after (b) thermal oxidation. All electrical transport measurements were performed in air at room temperature using a shielded probe station with triax connectors in order to minimize RF radiation noise. (See more details of SiNW device fabrication and transport measurements in ref 11.) After electrical characterization, cross section of each device was prepared with focused ion beam and imaged by HR-TEM to measure dimensions and examine morphology. Cross sections of the SiNWs showed a single-crystalline surface having a nearly circular and smooth profile with dimensions as low as ~3 nm. (See ref 11 for additional HR-TEM images and interfacial details.) In these SiNW FETs, two bias fields are provided from external sources: the transverse gate voltage applied to the back-gate electrode ($V_{BG}$) determines the effective width of the channel and the carrier density inside the channel, while the longitudinal drain–source voltage ($V_{DS}$) transports carriers through the channel body.

Quantum Confinement in 1D SiNW FETs. First, we identify quantum size effects in transfer characteristics of p-SiNW FETs. As illustrated in Figure 1, the channel body of ultrathin SiNW FETs is confined in both [001] (top) and [110] (sides) directions, so that motion normal to [110] is restricted physically by the SiNW channel body and the carriers (holes) are free to move only in the [110] direction, producing a series of quantized energy levels; each energy level forms a subband. Subband energies and hence intersubband structure depend strongly on the boundary conditions of quantum confinement, which is closely related to the cross sectional shape of NWs. Each sub-5 nm SiNW essentially forms a 1D system of electrons, since the diameter of the NWs is close to the wavelength of an electron (~10 nm). The corresponding 1D subband structure results in a series of sawtooth-like oscillatory DOS.4,15 (See Figure S1 in Supporting Information.)

As shown in Figure 2, the source–drain current $I_{DS}$ increases quasi-linearly at low back-gate voltage $|V_{BG}|$. However, when $|V_{BG}|$ is increased further, the channel current starts to increase superlinearly and several steplike and oscillatory structures are observed in drain current and transconductance, respectively. Clear shoulders or steplike structures are visible in drain current and transconductance, respectively.

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current spectrum shown in Figure 2 indicates that near-
threshold carrier conduction (|V_{BC}|~ few volts) occurs through
several subband channels.

Transfer characteristics of NW FETs with very dissimilar
cross sectional profile would be different, since quantum
confinement effects are closely related to channel boundary
conditions.15 (See Figures S2–S4 in Supporting Information
for more on transfer characteristics.) The dissimilarity between
the transconductance characteristics of Si-FETs patterned with
a NW (Figure 2) versus a NB (inset of Figure 2) is physically
plausible, recalling features in the DOS of the 1D versus 2D
structures. A Si FET consisting of a NW with a cross section of
4.3 nm \times 3.6 nm is essentially a 1D system with a sawtooth like
DOS but that of a NB with cross section of 4.3 nm \times 161 nm is
a quasi-2D system with stairlike DOS.14,15 (See Supporting
Information Figure S1 for the DOS.) Carrier confinement and
the corresponding DOS can result in oscillations in carrier
conductance and mobility. The transfer characteristics of the
NB FET (inset of Figure 2) show fast increase of I_{DS} with gate
voltage, while g_{M} shows uniformly increasing conductance
peaks with larger interpeak separation, which is an indication of
the stairlike 2D DOS profile resulting from the accumulated
contributions of individual 2D subband channels. Instead, the
characteristics of the NW FET reveal relatively quiet current
saturation accompanied with reduction of g_{M} for increasing gate
bias, implying behavior of inverse-square-root singular 1D DOS
at the bottom of each 1D subband. We also note that
geometrically narrower dimensions of “cylindrical” NWs result
in both nonuniformly spaced and larger subband separations,
but laterally confined NBs resemble a quasi-2D electron gas of
uniformly spaced subband structure (with increasing separa-
tions for higher subbands).15

**Channel Conductance Behavior and Intersubband
Spectroscopy.** Here, we identify quantum size effects in
channel conductance characteristics and related intersubband
separations in p-SiNW FETs. For a given value of V_{BC}, the
channel conductance, g_{D}(= \partial I_{DS}/\partial V_{DS}|_{V_{BG}=\text{const}},) also varies with
V_{DS}. (See Figure S5 in Supporting Information.) The periods of
repeated structures in I_{DS} can be obtained by analyzing g_{D}
in terms of V_{DS} and 1D intersubband separation can be
determined from the g_{D} characteristics with V_{DS}.18 Figure 3a
shows a contour representation of d_{g_{D}}/dV_{BG} at 300 K, as
functions of V_{DS} and V_{BG}. Patterns of strong oscillations in d_{g_{D}}/
dV_{BG} are clearly visible. The dark (blue) areas refer to the
regions of quickly increasing channel conductance, while light
(green) areas represent the regions of quickly decreasing
channel conductance. The zeros and high values of d_{g_{D}}/dV_{BG}
correspond to conductance plateaus and interplateau transition
regions in I_{DS}/V_{DS} curve. Figure 3b illustrates measured I_{DS}–
V_{DS} characteristics of a p-SiNW FET for various values of V_{BG}
at 300 K and corresponding g_{D}–V_{DS} (curves for V_{BG} = 0.3
and \approx 0.9 V shown). Strong oscillations in g_{D} with both biases
V_{DS} and V_{BG} are clearly seen with amplitude of oscillations
increasing at higher values of V_{DS} and V_{BG}. For I_{DS}–V_{DS} curves,
the V_{BG} is changed in \approx 0.2 V steps and the lowest trace in the
figure is for V_{BG} = \approx 0.3 V. In general, I_{DS} increases with V_{DS} and
V_{BG} because both the energy states for current flow and the
number of 1D conduction channels increase,16 and g_{D} shows
strong oscillation with increasing V_{DS}. In Figure 3b, stairlike
increase in I_{DS}(V_{DS}) is seen, and we find that the peaks in g_{D}
are nearly uniformly spaced. It is also apparent that the period of g_{D}
increases slightly as the magnitude of back-gate voltage V_{BG}
increases, implying that a higher gate field gives rise to further
confinement of the carriers in the channel body, leading to
increased separation between subbands; the transverse gate
field induces further confinement (“field-induced confine-
ment”) of the carriers in the narrow channel body.

From the g_{D}–V_{DS} curves at a given V_{BG}, the subband
separation \Delta E_{n+1,0} can be extracted. (See Supporting
Information Text S.) Let us consider the case of the equilibrium
chemical potential \mu_{0} (= E_{F}) located somewhere between
subband energies E_{n} and E_{n+1}. (See Supporting
Information Figure S1.) As V_{DS} is increased slowly, I_{DS}
remains constant staying on the same plateau, waiting until either \mu_{0}
gets equal to E_{n+1} (V_{DS}) or \mu_{0} equals to E_{n+1} (V_{DS}) at V_{DS}
so that a new subband channel opens and I_{DS} increases to a new value I_{DS}.
On increasing V_{DS} extremal in g_{D}(V_{DS}) can occur at characteristic values of V_{DS}. If we let the two nearest maxima
of g_{D}(V_{DS}) occur at the drain voltages V_{1} and V_{2} the
corresponding intersubband separation is given by \Delta E_{n+1,0} =
\Delta V_{DS} with \Delta V_{DS} = V_{2} – V_{1}.19 Therefore, the period of peaks,
\Delta V_{DS} corresponds to the subband separation of the channel.
body. From the $g_0(V_{DS})$ behavior in Figure 3b, we obtain $\Delta E_{m1,n0} \sim 65 \pm 10$ meV for the low-lying few subbands in the p-SiNW FET with cross section of 4.3 nm × 5.7 nm. Remembering that the subband separation increases with the channel radius,15 our experimental value of 65 ± 10 meV is in accord with a theoretical prediction of ~50 meV for p-SiNW FET of 5 nm × 5 nm cross section.20 For an order-of-estimation of subband separations in SiNWs, let us take a p-SiNW body as an infinitely confined cylindrical 1D electron system of radius $r_0$ treating gate oxide as an infinite potential barrier to Si channel body even though the valence-band offset of SiO$_2$–Si is ~4.5 eV.21 The lowest two subband separations $\Delta E_{n0,n+1}$ are 58.1 and 53.1 meV if we use 2$r_0$ = 5 nm for NW diameter (71.8 and 65.6 meV if we use 2$r_0$ = 4.5 nm) and $m^* = 0.15 m_0$ of light-hole effective mass in the [110] direction, where $m_0$ is the free-electron mass. (See Supporting Information Text 3.) The lowest hole subband is of light holelike character.20 This order-of-magnitude estimation of intersubband separation is also in agreement with our experimentally extracted value ($\Delta E_{m1,n0} \sim 65 \pm 10$ meV) for low-lying subbands in our p-SiNW FET. This extracted subband separation at 300 K corresponds to $\Delta E_{m1,n0} \simeq (1.7 \pm 0.24) k_B T$ or in terms of thermal energy to $\Theta = 510 \pm 72$ K, which is about one-half of the theoretical thermal broadening criterion ($\Delta E = 3.5 k_B T$) for clear resolution of quantum oscillations in mesoscopic transport measurements.2,22 Hence, the presence of measurable quantum oscillatory behavior in our p-SiNW FETs at room temperature is well justified.

Confinement-induced quantum oscillatory behavior is known to be observable provided that the source–drain bias $eV_{DS}$ is not much larger than subband separation $\Delta E_{m,n}$. For small $V_{DS}$ nearly flat and parallel subband channels are expected to produce clear oscillations in source–drain transfer characteristics as far as $eV_{DS}$ is not much larger than a few times the intersubband separation $\Delta E_{m,n}$.17 Under a strong source–drain bias field, the confinement potential is greatly tilted down along the channel by the drain bias such that the gate field can induce more carriers easily. When the chemical potential at the drain side $\mu_D$ is pulled down drastically, the effective channel length is significantly reduced and, as a result, the quantum mechanical interference effect can be visible in transport parameters such as conductance and mobility of short-length SiNW FETs in the quasi-ballistic regime.17,23,24 Park et al. also report enhanced drain current oscillations in inversion mode of their Si FET for high $V_{DS}$ albeit at low temperature.25 (See Figure 3 in ref 25.) Nevertheless, the continuing (sometimes much enhanced) oscillatory behavior in $I_{DS}–V_{BG}$ and $g_0–V_{BG}$ at higher $V_{DS}$ in our p-SiNW FETs is not fully understood yet. (See Supporting Information Figure S5.) One possible source of this observed effect could be related to strong electric field-induced intersubband scattering near the drain.25 We suppose that extremely nonequilibrium high field dielectric response would be responsible for the persisting oscillatory behavior at high drain–source electric field,27 and more rigorous analysis such as nonequilibrium Green function approach to quantum transport equations28 would provide microscopic understanding of carrier transport characteristics of such ultrathin quantum devices.

**Field-Effect Mobility Behavior of SiNW FETs.** Here, we identify quantum size effects in carrier mobility of p-SiNW FETs. Field-effect mobility ($\mu$) of conventional MOSFETs is written as $\mu = (g_M L)/(V_{DS} C_W W)$, where $L$, $W$, and $C_W$ ($\equiv C/(LW)$) are the gate length, width, and the gate oxide capacitance per unit area, respectively. Therefore, mobility characteristics should also show oscillatory behavior with respect to gate voltage, similar to $g_M$ of the SiNW FETs. For reliable determination of $C_W$, finite element mesh simulation was performed using COMSOL package with the specific geometry of each device, as measured by HR-TEM imaging.11 Our simulated capacitance gives $C_W \approx 4.0$ mF/m$^2$. Mobility characteristics of p-SiNW FETs are shown in Figure 4 in terms of $W_{BG}$ with $V_{DS} = 50$ mV at 300 K. Figure 4a shows $\mu$ of p-SiNW FETs for channel lengths of 2, 3, and 10 $\mu$m. In obtaining the mobility curves shown in Figure 4, we used $C = 4.15 \times 10^{-17}$ F, $6.22 \times 10^{-17}$ F, and $2.05 \times 10^{-16}$ F for channel length 2, 3, and 10 $\mu$m, respectively. The mobility shows clear oscillatory behavior with $V_{BG}$ similar to $g_M$. The periodic character of the 1D DOS is directly reflected as the periodic oscillation in carrier mobility of the SiNW FETs through the simple relation $\mu \propto 1/\sqrt{\Delta}$, where $1/\sqrt{\Delta}$ is some effective scattering rate. Decrease (increase) in $\mu$ with $|V_{BG}|$ corresponds to increase (decrease) in the DOS. As the gate bias increases, gradual occupancy of additional subbands by carriers results in increase of drain current and the steepest current increase (and, hence, a mobility peak) occurs when a new subband channel opens up for carrier transport; the oscillatory behavior occurs when carriers must “wait” for the

**Figure 4.** Field-effect mobility characteristics of Si FETs of various channel lengths and widths at 300 K. (a) Channel length dependence for three different NW devices with nanowire height of 4.3 nm and width of ~5.7, 5.1, and 3.6 nm for channel length of 2, 3, and 10 $\mu$m, respectively. (b) Comparison of mobilities in NW and NB devices of 3 $\mu$m length. The widths of NW and NB devices are 5.1 and 161 nm, respectively.
Fermi level in the channel to rise to include the subsequent subband. Figure 4a shows that peak mobility occurs at relatively low gate biases near $V_{BG} \sim 2 \text{ V}$, and the overall mobility is enhanced in the NW devices with longer channel body. Although the NW device with 10 μm long channel body shows reduced transconductance behavior (as illustrated in Figure S2 in Supporting Information), it produces the highest peak mobility value, approaching over $\sim 900 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. This apparent feature is attributed to the fact that relative carrier mobility of various SiNW FETs is controlled by the product of $g_{SO}(L/W)$, since the remaining factor, $V_{DS}C_{ox}$ in the expression $\mu = (g_{SO}C_{ox})/((V_{DS}C_{ox}W)$ is independent of channel cross sectional dimensions; for example, $L/W$ is largest for the 10 μm long nanowire device due to long length and smallest NW cross section. The fact that $g_{SO}$ does not scale proportionally with $(L/W)^{-1}$ implies an intrinsic increase of mobility in nanowires with a smaller cross section, like the 4.3 nm × 3.6 nm NW device in Figure 4a (also see Figure S2 in Supporting Information). Figure 4b shows field-effect mobility characteristics of 3 μm long SiNW FET with cross section of 4.3 nm × 5.1 nm and SiNB FET with cross section of 4.3 nm × 161 nm. The disparity in gate bias dependence of field-effect mobility in NW FETs as compared to NB FETs resembles the corresponding disparity in transport and transconductance characteristics of the two devices seen in Figure 2. (See also Figure S4 in Supporting Information.) The overall performance of SiNW and SiNB devices is distinctive due to the unique DOS of respective device. For the SiNB FET, the mobility continues to oscillate with $V_{BG}$, revealing uniformly spaced peaks, which is an indication of the ladderlike accumulated DOS profile of 2D subband channels. In contrast, mobility behavior of the SiNW FET discloses (more clearly at low gate bias fields) the behavior of inverse-square-root singularities at the bottoms of each 1D subband. At high gate bias, average mobility is considerably reduced in NW devices, as more subband channels are opened for carrier transport at higher gate bias, due to increased intersubband scattering caused by larger variation in effective mass of carriers in different subband. We confirm that higher mobility values observed in our SiNW devices arise from enhanced intersubband separation in ultrathin conduction channel bodies as well as improved structural perfection and cylindrical morphology. Therefore, quantum confinement-induced enhancement in hole mobility justifies the recently reported higher performance in p-SiNW FET devices.

Carrier mobility can strongly be influenced by acoustic phonon scattering. The carrier-acoustic phonon scattering rate can be estimated employing deformation potential theory along with the Fermi golden rule. For a SiNW FET of 5 nm diameter and of $E_g = 10 \text{ meV}$, we estimate the acoustic scattering time $\tau_{ac} \sim 8.7 \times 10^{-12} \text{ s}$ at 300 K. (See Supporting Information Text 6.) Using $\tau_{ac} \sim 8.7 \times 10^{-12} \text{ s}$ and $\nu_f (= 2E_g/m^*)^{1/2} \approx 1.5 \times 10^6 \text{ m/s}$, one can calculate the mean free path for carriers of light-hole mass to be $l_{ac} \sim 1.3 \mu\text{m}$. In sub-5 nm Si[110] NW FETs, the lowest two hole subbands are nearly two-fold degenerate light-hole mass so that phonon-assisted intersubband scattering can be neglected within these two nearly degenerate subbands. Furthermore, considering Si Debye energy of 55 meV and significantly enhanced intersubband separation ($\Delta E_{SO} \approx 55-75 \text{ meV}$) in sub-5 nm ultrathin SiNW FETs, acoustic phonon assisted intersubband scattering is expected to be rather minimal between the subsequent low-lying subband channels. All these features would clearly give rise to a boost in field-effect hole mobility in our p-SiNW FETs. Our observation is in line with theoretical predictions of enhanced hole mobility in strongly confined NWs. Since the carrier relaxation time is inversely proportional to the DOS, relaxation time $\tau(E)$ should also reveal oscillatory behavior because of the periodic inverse-square-root singular enhanced DOS at the 1D subband edges of the channel body. Although our analysis of carrier-acoustic phonon scattering rate is macroscopic, this estimation of low scattering rate is also in support of quantum oscillatory transport behavior (oscillatory behavior lends to high peak performance through unique DOS) in our sub-5 nm SiNW FETs persisting at room temperature. Surface roughness scattering could potentially be significant in such small nanowires. However, we expect it to be minimal because thermal oxidation on plasma etched NWs evidently reduces sidewall roughness. Furthermore, as these FETs are back-gated, the carriers would be confined away from the possibly imperfect top oxide-Si interface. Impurity scattering is expected to be negligible due to low doping and reduced volume of ultrathin nanowire devices. We suppose the carriers are physically scattered mostly at the metallic source and drain contacts in our junctionless devices. Additionally, reduced carrier effective mass in an ultrathin SiNW channel body also constitutes enhanced performance (through reduced acoustic phonon assisted intersubband carrier scattering) for transport within the SiNW FETs.

In summary, we have presented evidence of confinement-induced quantum oscillatory behavior prevailing at 300 K in drain-source current, transconductance, and field-effect mobility characteristics of ultrathin top-down fabricated SiNW FETs. Effects of quantum confinement on channel conductance and transconductance are described in terms of quantized 1D subband structures and the corresponding unique 1D DOS. Carrier mobility characteristics are shown to differ depending on the cross sectional geometry of the channel body, such that disparity in mobility characteristics of SiNW and SiNB devices resemble the corresponding disparity in transfer conductance characteristics of the drain-source current.

We conclude that strongly enhanced peak field-effect mobility in p-SiNW FETs results from the unique 1D DOS of inverse-square-root singularity. Ambient operation of SiNW devices with cross sectional dimensions of sub-5 nm scales should be understood in terms of quantum aspects of strongly confined carriers. As such, this study would serve as a guide for basic understanding of physical characteristics of nanoelectronics devices consisting of ultrathin SiNW FETs as potential key building blocks for future electronics devices. We believe quantum confinement effects are a key avenue to unlock performance and extend scalability of future Si technology as well as foster new applications of Si devices.

**ASSOCIATED CONTENT**

**Supporting Information**

Additional information regarding (1) carriers in confined structures, (2) channel length- and width-dependences of transfer characteristics, (3) intersubband separations in cylindrical nanowires, (4) channel conductance behavior with the gate- and channel-bias voltages, (5) subband spectroscopy, and (6) carrier-acoustic phonon scattering rate and mean free path. This material is available free of charge via the Internet at http://pubs.acs.org.
**REFERENCES**

Supporting Information file: Text and Figures

Text 1: Carriers confined in confined structures

In our ultra-thin devices, carrier transport deviates significantly from predictions in classical device physics. The unexpected behavior of conductance and mobility can be understood in terms of the density of states (DOS) in the device. Figure S1 illustrates the 1D subband structure (left panel) and the density of states (right panel) in a Si nano wire (SiNW) channel body. The lowest five subband bottom energies, $E_n$, with n=1, 2, 3, 4, and 5 and the nonequilibrium chemical potentials, $\mu_S$ and $\mu_D$, at the source and drain electrodes are illustrated. The equilibrium chemical potential is $\mu_0$. The 2D density of states is indicated by dotted lines on the right panel.

Figure S1. Schematics of 1D subband structure and density of states. (a) 1D subband structure. The lowest five subband bottom energies $E_n$ with n=1, 2, 3, 4, and 5 and the non-equilibrium chemical potentials, $\mu_S$ and $\mu_D$, at the source and drain electrodes are illustrated, and $\mu_0$ is the equilibrium chemical potential. (b) Density of states. The 2D density of states is indicated by dotted lines on the right panel.
The DOS per unit length in a 1D system is written as
\[ D_{\text{1D}}(E) = \frac{1}{\pi} \sqrt{\frac{2m^*}{\hbar^2}} \sum_{n,m} \Theta(E - E_{nm}). \]
Here, the spin degeneracy of 2 is assumed, and \( \Theta(x) \) and \( E_{nm} \) denote the Heaviside function and the 1D subband bottom energy, respectively. (We note that the energy of a carrier in a 1D subband is given by
\[ E_{nm}(k) = E_{nm} + \frac{\hbar^2 k^2}{2m^*}, \]
where \((n,m)\) are the subband quantum numbers for a system of 2D confinement.)

As the energy \( E \) approaches the subband bottom \( E_{nm} \), the 1D DOS shows spike-like singular behavior, which repeats for all the quantized subband channels. SiNWs of sub-5 nm diameter are essentially 1D semiconductors since the diameter of the NWs are close to the de Broglie wavelength of a carrier \((\lambda_F \sim 30 \text{ nm} \text{ for light holes of } m^* = 0.15 m_0 \text{ at } E_F \approx 10 \text{ meV in a typical SiNW of 5 nm radius})\).

Therefore, the DOS of neighboring subbands are well separated from each other due to the large subband separations. As \( |V_{BG}| \) is raised above the threshold voltage \( V_{BG}^{\text{Th}} \), the Fermi level \( E_F \) traverses subband bottoms and the DOS at the Fermi energy \( D(E_F) \) becomes significantly reduced in between neighboring subband bottoms. The sharply reducing \( D(E_F) \) results in saturation of source-drain current \( I_{DS} \) until a higher-lying subband (with the next singular peak of DOS) begins to be populated. This occurs repeatedly as gate voltage is increased, thereby showing repeated structures as more subbands are populated by carriers. This feature can be observed in transport measurements such as the drain current \( I_{DS}(V_{BG}) \), channel conductance \( g_D \), transconductance \( g_M \), and carrier mobility of the NWs. In contrast, the density of states is stair-like in a 2D system and is written, normalized to the unit area, as
\[ D_{\text{2D}}(E) = \frac{m^*}{\pi \hbar^2} \sum_{n} \Theta(E - E_n). \]
When the width of a device is significantly larger than its height, as in the case of nano belts (NBs), the 2D DOSs behavior would be demonstrated in the transfer conductance or carrier mobility characteristics. As the energy value \( E \) overtake each subband bottom energy \( E_{nm} \), the 2D DOS shows a stair-like jump to give a ladder-like total DOS (dotted lines on the right panel in Supporting Fig. S1) covering over all the quantized subband channels.
In SiNW FETs, carrier transport can only occur in NW bodies if subband states lying between the chemical potentials $\mu_S$ and $\mu_D$ of the source and drain are available. In order to have hole carriers conduct through the channel, filled electron subband states are required to be available around the chemical potential ($E = \mu_0$) before a drain voltage $V_{DS}$ is applied. In the presence of a finite bias field between source and drain electrodes, the carrier Fermi level is not constant any more in the device, and the source-drain current $I_{DS}$ derives from carriers in the energy interval $[E_F - eV_{DS}/2, E_F + eV_{DS}/2]$ ($=[\mu_D, \mu_S]$) due to the shifted chemical potentials from the equilibrium value $\mu_0 = E_F$. Here $\mu_S$ and $\mu_D$ are the non-equilibrium chemical potentials in the source and drain contacts, respectively, and a symmetric voltage drop $V_{DS}$ with $\mu_S - \mu_D = eV_{DS}$ is assumed, for simplicity. (See Fig. S1.) The energy window $[\mu_D, \mu_S]$ for current flow can be tuned by applying a source-drain bias $V_{DS}$ such that $eV_{DS} = \mu_S - \mu_D$, while we recall that $\mu_S$ and $\mu_D$ can be adjusted by a back-gate electrode bias $V_{BG}$. Therefore, both $V_{DS}$ and $V_{BG}$ determine which subbands comprise the overall current flow in a device.
Figure S2. Transfer characteristics of p-SiNW FET. Channel length dependence are shown, at 300 K with source-drain bias of 50 mV, for three different NW devices having NW height of 4.3 nm and width of ~5.7, 5.1, and 3.6 nm for channel length of 2, 3 and 10 μm, respectively. The data are of p-MOS devices; the horizontal axis is shown as a magnitude of back-gate voltage for convenience.

Text 2: Channel length- and width dependences of transfer characteristics

In Fig. S2, we show the channel length dependence of the transfer characteristics of p-SiNW FETs of ultra-thin cross section, with source-drain bias of 50 mV at 300 K. The results are illustrated for three different channel lengths 2, 3, and 10 μm, each with NW height of 4.3 nm and width of ~5.7, 5.1, and 3.6 nm, respectively. As the length of the channel body increases, the positions of transconductance peaks shift slightly towards lower back-gate bias voltage, but the corresponding inter-peak separation $\Delta |V_{BG}|$ remains the same for different body length, indicating that the 1D DOS is independent of the system length. The gate oxide capacitance increases weakly with body length. Our SiNW FET with of narrow cross section is essentially a 1D system, while the SiNB FET with cross section of 4.3 nm x 161 nm is a quasi 2D system of stair-like DOS. Depending on the cross sectional dimension of the channel, the transfer characteristic are different.
In Fig. S3, we display the channel length dependence of electrical resistance for our junctionless SiNW devices. The total resistance would be the sum of the source/drain contact \( R_{SD} \), channel \( R_{CH} \), and parasitic resistances. We note that in these junctionless devices, only contact and channel resistances are dominant contributors to total series resistance. By extrapolating the resistance at zero channel length \( (L=0) \) in Fig. S3, we surmise that the remaining \( R_{SD} \) is only a small fraction of total series resistance in our ultra-thin SiNW FETs. In conventional devices, one would expect that the channel resistance scales linearly with channel length - at least in channels long enough to exhibit steady-state transport after a spatially short initial transient. In our ultra-thin SiNW devices, the total resistance should be dominated by the channel resistance in longer channels, not so in shorter channels (in the limit of no channel, one would see only the source/drain contact resistance.)
**Figure S4.** Transfer characteristics of 3 μm Si FETs at 300 K. SiNW FET has cross section of 4.3 nm x 5.1 nm NW and SiNB FET has cross section of 4.3 nm x 161 nm. $V_{DS}$ is 50 mV. The data are of p-MOS devices; the horizontal axis is shown as a magnitude of back-gate voltage for convenience.

**Figure S4** illustrates the transfer characteristics of a 3 μm long SiNW FET and SiNB FET of cross sections 4.3 nm x 5.1 nm and 4.3 nm x 161 nm, respectively, for source-drain bias of 50 mV. The transfer characteristics of the source-drain current $I_{DS}(V_G)$ for the SiNB FET, at low gate voltages, show fast increase of drain current $I_{DS}$ with gate voltage $|V_{BG}|$. The nearly uniformly spaced conductance peaks (in transconductance) are an indication of the ladder-like DOS profile resulting from the accumulated contributions of individual 2D subband channels. On the other hand, the transfer characteristics of the SiNW FET, at low gate voltages, reveals relatively quick current saturation accompanied with concurrent reduction of transconductance, implying inverse-square-root singularities at the bottom of each 1D subband. Therefore, the difference between the transfer characteristics of SiNW and SiNB FETs displayed in Fig. S4 is physically plausible recalling the difference in the DOS of 1D and 2D systems.
Text 3: Intersubband separations in cylindrical nanowires

One can estimate an order-of-magnitude of the subband structure in a p-SiNW FET by approximating the channel body as a cylindrical SiNW surrounded by oxide (see TEM images shown in Fig. 1). Let us assume that the real SiNW can be modeled with a quasi-1D NW of length $L$, in which carriers propagate freely along the wire; the transverse motions (in the y and z directions) are quantized into discrete 2D subbands due to finite confinement potential $U(\approx 4.5$ eV), originating from the valence-band gap mismatch between the SiNW and gate oxide. Let the wire have a circular cross section of radius $r_0$, and, for further simplicity, we consider gate oxide providing an infinite potential barrier to the channel body such that $U = \infty$. Then, the quantum mechanical states of the carriers in the NW are described, in terms of the three quantum numbers $(n, \ell, k)$, by $\Psi_{n,\ell}(k,r)$. Here $n = 1, 2, 3, \ldots$, $\ell = 1, 2, 3, \ldots$, and $k$ is the wave number of the carriers along the NW axis. Corresponding subband energies are given by

$$
E_{n,\ell}(k) = \frac{\hbar^2}{2m^*} \left[ k^2 + \frac{\chi_{n,\ell}^2}{r_0^2} \right],
$$

where $m^*$ is the carrier (hole) effective mass along the channel, and $\chi_{n,\ell}$ denotes the dimensionless parameter representing the $\ell$th zero of the Bessel function of order $n$:

$$
J_n(\chi_{n,\ell}) = 0.
$$

The first few roots $\chi_{n,\ell}$ of the equation $J_n(r) = 0$ can be found in a standard mathematical handbook. Now, subband separations are given by

$$
\Delta E(n'\ell';n\ell) = \frac{\hbar^2}{2m^*r_0^2}(\chi_{n',\ell'}^2 - \chi_{n,\ell}^2).
$$

We note that subband separations are inversely proportional to the product of the carrier effective mass and the size of the 1D channel body cross section. As the channel diameter increases, the intersubband separation $\Delta E(n'\ell';n\ell)$ decreases such that quantum confinement effects are diminished. Since the Bessel function oscillates with non-uniform periods, the zeros of a given Bessel function are not uniformly distributed. Therefore, in an infinitely confined cylindrical NW, 1D intersubband separations are neither constant nor varying in a simple form. The lowest 6 subband states $\Psi_{n,\ell}$ are $\Psi_{01}$, $\Psi_{11}$, $\Psi_{21}$, $\Psi_{02}$, $\Psi_{31}$, and $\Psi_{12}$ and the corresponding subband separations $\Delta E(n'\ell';n\ell)$ are given by

$\Delta E(11;01) = 58.1$ meV, $\Delta E(21;11) = 53.1$ meV, $\Delta E(02;21) = 15.7$ meV, $\Delta E(31;02) = 35.0$ meV, and
\[ \Delta E(12;31) = 25.9 \text{ meV} \]

if we use \( 2r_0 = 5 \text{ nm} \) for NW radius and \( m^* = 0.15 \ m_0 \) for light-hole effective mass in the [110] direction, where \( m_0 \) is the free-electron mass. The lowest hole subband is assumed of light hole-like character.\(^7\) (If we take \( 2r_0 = 4.5 \text{ nm} \) and \( m^* = 0.15 \ m_0 \), we expect

\[ \Delta E(11;01) = 71.8 \text{ meV}, \ \Delta E(21;11) = 65.6 \text{ meV}, \ \Delta E(02;21) = 19.3 \text{ meV}, \ \Delta E(31;02) = 43.3 \text{ meV}, \ \text{and} \ \Delta E(12;31) = 32.0 \text{ meV}. \)

Although the assumption of infinite confinement potential overestimates the subband energy separations, the present order-of-magnitude estimation of intersubband separation is in accord with our experimental data \( \Delta E_{n+1,n} = 55 – 75 \text{ mV} \) for low-lying few subbands in our 2\( \mu \text{m} \) long p-SiNW. Under back-gated bias, carrier conduction occurs closer to the interface with buried oxide, and the ‘effective cross section’ of the carrier conduction channel becomes smaller than the physical cross section of the NW. This reduced channel geometry gives rise to enhanced intersubband separations.

**Text 4: Channel conductance behavior with the gate- and channel-bias voltages**

**Figure S5** shows channel conductance \( g_D \) as a function of back-gate voltage \( V_{BG} \) for a p-SiNW FET with cross section 4.3 nm x 5.7 nm and channel length 2 \( \mu \text{m} \) at room temperature. On the whole, \( g_D \) decreases gradually as negative gate voltage \( V_{BG} \) approaches 0 for small values of \( V_{DS} \) (< 0.1 V), but \( g_D \) shows oscillatory behavior at enhanced source-drain voltages \( V_{DS} > 0.1 \text{ V} \). The lowest trace is at \( V_{DS} = 25 \text{ mV} \), and successive traces for \( V_{DS} \geq 50 \text{ mV} \) are offset in the vertical direction for clarity and show the evolution of channel conductance as \( V_{DS} \) is increased by 25 mV successively up to \( V_{DS} = 225 \text{ mV} \). Weak shoulder-like features are repeated at low values of channel bias \( V_{DS} \), and we attribute this feature in \( g_D \) to gradual occupancy of additional subbands by carriers to transport through the channel (quasi-coherently) for the range of \( V_{DS} < 100 \text{ mV} \).
Text 5: Subband Spectroscopy

The transport properties of the 1D channel body are strongly influenced by the 2D confinement potential $U$, which depends not only on the channel configuration but also the external bias voltages $V_G$ and $V_{DS}$, that is, $U = U(V_G, V_{DS})$. The gate voltage $V_G$ determines the effective channel width and the carrier density of the NW, and the change in confinement potential $U$ is not identical to the changes in the external gate bias $V_G$. On the other hand, $V_{DS}$ is the bias potential between the source and drain reservoirs of the device. In the sub-threshold region, the source to drain current $I_{DS}$ is controlled by both the source-drain voltage $V_{DS}$ and gate voltage $V_G$, because both $V_{DS}$ and $V_G$ induce modulation of the SiNW band edge alignments in the channel body. By applying a voltage difference $V_{DS}$ between the two reservoirs, a current can be induced through the NW. Finite value of channel bias $V_{DS}$ shifts the

Figure S5. Channel conductance of a p-SiNW FET for various source-drain biases at 300 K. The NW FET has cross section of 4.3 nm x 5.7 nm and channel length 2 μm. The lowest trace is at $V_{DS}=25$ mV, and successive traces (offset in the vertical direction for clarity for $V_{DS} \geq 50$ mV) show the evolution of channel conductance as $V_{DS}$ is increased in 25 mV steps up to $V_{DS}=225$ mV.
chemical potentials at the source (drain) electrodes up (down) and induces a current to flow through the device. The influence of $V_{DS}$ on $\mathcal{U}$ resembles the role of ordinary external gate field and hence termed ‘self-gating’.\textsuperscript{9} At finite temperature $T$, a current can flow only when the subband states are located within a few $k_BT$ around the $\mu_S$ and $\mu_D$. When the carrier energy is increased above the lowest subband bottom at the source side, carriers begin to flow into the channel body. In a back-gated device, holes in the positive wave number states transport towards the source electrode. For further increase of carrier energy, higher lying subband states are successively occupied by carriers and additional conduction channels are opened in the device. Then, the spin-degenerate total electric current $I_{DS}$ can be expressed as\textsuperscript{10,11}

$$I_{DS}(V_{DS}, T) = 2\frac{e}{h} \sum_n \int_{-\infty}^{\infty} d\varepsilon \mathcal{T}_n(\varepsilon) \Delta f(\varepsilon + E_n).$$

Here $\mathcal{T}_n(\varepsilon)$ and $\Delta f(\varepsilon)$ are, respectively, the transmission coefficients $\mathcal{T}_n(\varepsilon) \equiv \mathcal{T}_n[\varepsilon, \mathcal{U}(V_G, V_{DS})]$ and $f(\varepsilon - \mu_S) - f(\varepsilon - \mu_D)$, the occupation difference for the source and drain contacts of the channel body, where $f$ is the Fermi-Dirac distribution function $f(\varepsilon - \mu) = 1/[e^{(\varepsilon - \mu)/k_BT} + 1]$. We have noted that the positive and negative velocity components are determined, respectively, by the chemical potential $\mu_S(= \mu_0 + \frac{1}{2}eV_{DS})$ at the source side and the chemical potential $\mu_D(= \mu_0 - \frac{1}{2}eV_{DS})$ at the drain side of the channel, and $\Delta f(\varepsilon) \approx \frac{\partial f}{\partial \varepsilon} eV_{DS}$ for small drain bias. (See Fig. S1.) As additional conduction subband channels are opened, the transmission coefficient would show step-like increase with gate or channel bias fields. One can formally write $I_{DS}$ as

$$I_{DS} = I[\mathcal{U}(V_G, V_{DS}), \Delta f(V_{DS})]$$

to express $g_M(\equiv \frac{\partial I_{DS}}{\partial V_G}$ at constant $V_{DS}$) and $g_D(\equiv \frac{\partial I_{DS}}{\partial V_{DS}}$ at constant $V_G$), respectively.

The channel conductance $g_D$ is evidently a measure of current contributions from the carriers of energy close to the two electrochemical potentials $\mu_S$ and $\mu_D$, because $\frac{\partial f}{\partial \varepsilon}$ is mostly significant at the energy values close to the chemical potentials, especially at low temperatures. Because the confinement
potential $U$ can be controlled either by the gate bias $V_G$ or the source-drain bias $V_{DS}$, one can extract information about the 1D subband structures by sweeping the bias fields across the channel and obtaining the channel conductance $g_D$ of the device. Here, let us focus first on the finite source-drain bias spectroscopy, in which $g_D$ is determined by sweeping a dc source-drain bias voltage $V_{DS}$ across the NW body. The $I_{DS}(V_{DS})$ curve, for a given gate bias, would disclose abrupt change in slope whenever the increased $V_{DS}$ pulls down $\mu_D (= \mu_0 - \frac{1}{\hbar} eV_{DS})$ until it lies below the lowest subband bottom energy. Once $\mu_D$ lies below the lowest subband bottom energy, the channel conductance would show saturated drain current $I_{DS}$. $^{12}$ We recall that under back-gated bias, the carrier conduction would occur closer to the interface with buried oxide, and the ‘effective cross section’ of the carrier conduction channel becomes smaller than the physical cross section of the NW. We suppose that our observation of increased inter-peak separations at higher gate voltages is in accord with enhanced intersubband separations caused by further confinement (i.e., reduced effective channel cross section) induced by higher gate fields. This reduced channel geometry also enhances carrier mobility through subsequent reduced interfacial scattering.

**Text 6: Carrier-acoustic phonon scattering rate and mean free path**

As the gate voltage increases beyond threshold values for successive subband occupancy, carriers can scatter into neighboring subband states with the help of ambient phonons, which would induce fluctuations in transfer conductance and mobility decrease. However, in ultra-thin NW 1D structures, the carrier-lattice scattering processes is expected to be greatly suppressed due to highly restrictive conservations of momentum and energy, giving rise to enhanced lifetimes and mean free paths for carriers in the system. Moreover, drastically increased subband separation, in strongly confined SiNW FETs, would make it difficult for a carrier in a given subband state to scatter into another subband state in close proximity through carrier-phonon assisted intersubband scattering.
Typically, carrier mobility can be strongly influenced by acoustic phonon scattering. As the gate voltage is increased beyond threshold values for successive subband occupancy, carriers can scatter into neighboring subband states with the help of ambient phonons, which would induce fluctuations in transfer conductance and mobility degradation. In a NW, carrier-acoustic phonon scattering is suppressed due to the reduced phase space available for final states back scattering. In sub-5nm Si [110] NW FETs, the highest valence subband is nearly two-fold degenerated light-hole like, so that phonon assisted intersubband scattering can be avoided. In addition, taking into account the bulk Si Debye energy of 55 meV and significantly enhanced intersubband separation (ΔE_{n,n+1} ~ 55−75 meV) in sub-5nm thin SiNW FETs, the acoustic phonon assisted intersubband scattering is also expected to be rather minimal between the low-lying subband channels. In ultra-strongly confined NW structures, the carrier-carrier and carrier-lattice scattering processes are greatly suppressed due mainly to highly restrictive conservations of momentum and energy, giving rise to enhanced lifetimes and mean free paths for carriers in the system. These factors would clearly give rise to a significant boost in low-field hole mobility, as is observed in our p-SiNW FETs. Hence, our observation is in line with theoretical predictions of enhanced hole mobility in strongly confined NWs.\(^{14}\)

Let us consider the case that carriers are scattered at the acoustic phonon induced lattice deformations.\(^{15,16}\) The carrier-acoustic phonon scattering rate can be estimated by means of the Fermi golden rule, and is given by\(^{17}\) \(\frac{1}{\tau_{ac}} = \frac{\pi k_B T \Xi^2}{\hbar\rho v_s^2} \tilde{D}(E_F).\) Here \(\rho, v_s, \tilde{D}(E_F),\) and \(\Xi\) are, respectively, the SiNW mass density, the longitudinal sound velocity, the 1D DOS (normalized to unit area) at the Fermi energy, and the deformation potential representing the coupling of the carrier to longitudinal acoustic phonons. For a NW of radius \(r_0,\) \(\tilde{D}(E_F)\) is written as \(\tilde{D}(E_F) = \frac{1}{\pi \hbar} \sqrt{\frac{2m^*}{E_F}} \frac{1}{\pi r_0^2}.\) Now, one can estimate relaxation time \(\tau_{ac}\) using the above expressions. If we choose the following material parameters, for example: acoustic deformation potential \(\Xi = 1.88\) eV, \(\rho = 2.33\) g/cm\(^3\),
\[ \nu_s = 9000 \text{ m/s}, \quad m^* = 0.15 \, m_0 \text{ (light hole mass)}, \quad r_0 = 2.5 \text{ nm}, \quad E_F = 10 \text{ meV}, \quad \text{and} \]

\[ \tilde{D}(E_F) = 2.0 \times 10^{45} / \text{J} \cdot \text{m}^3 \text{ for our SiNW FET of 5 nm diameter}, \]

we estimate the acoustic scattering time \( \tau_{ac} \approx 8.7 \times 10^{-12} \text{ s at 300 K}. \) Using \( \tau_{ac} \approx 8.7 \times 10^{-12} \text{ s} \) and \( \nu_s (\approx \sqrt{2E_F / m^*}) \approx 1.5 \times 10^5 \text{ m/s}, \) one can obtain the mean free path for carriers of light hole mass to be \( \ell_{ac} \approx 1.3 \mu \text{m}. \) This is a direct result of narrow cross sectional dimensions of sub-5 nm and the square-root singular enhanced density of states at the 1D subband edges of the channel. Along with reduced trap density at the Si-oxide interface, thermal oxidation on plasma etched SiNWs evidently plays a key role in reducing surface roughness scattering in our NW FETs. In addition to reduced impurity and surface roughness scatterings, reduced carrier effective mass and increased subband separations in the ultra-thin SiNW channel body apparently give rise to an enhanced mobility for transport within the SiNW FET.

References for Supporting Information


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potential $U$ can be controlled either by the gate bias $V_G$ or the source-drain bias $V_{DS}$, one can extract information about the 1D subband structures by sweeping the bias fields across the channel and obtaining the channel conductance $g_D$ of the device. Here, let us focus first on the finite source-drain bias spectroscopy, in which $g_D$ is determined by sweeping a dc source-drain bias voltage $V_{DS}$ across the NW body. The $I_{DS}(V_{DS})$ curve, for a given gate bias, would disclose abrupt change in slope whenever the increased $V_{DS}$ pulls down $\mu_D (= \mu_0 - \frac{1}{2} e V_{DS})$ until it lies below the lowest subband bottom energy. Once $\mu_D$ lies below the lowest subband bottom energy, the channel conductance would show saturated drain current $I_{DS}$. We recall that under back-gated bias, the carrier conduction would occur closer to the interface with buried oxide, and the ‘effective cross section’ of the carrier conduction channel becomes smaller than the physical cross section of the NW. We suppose that our observation of increased inter-peak separations at higher gate voltages is in accord with enhanced intersubband separations caused by further confinement (i.e., reduced effective channel cross section) induced by higher gate fields. This reduced channel geometry also enhances carrier mobility through subsequent reduced interfacial scattering.

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Here \(\rho\), \(v_s\), \(\tilde{D}(E_F)\), and \(\Xi\) are, respectively, the SiNW mass density, the longitudinal sound velocity, the 1D DOS (normalized to unit area) at the Fermi energy, and the deformation potential representing the coupling of the carrier to longitudinal acoustic phonons. For a NW of radius \(r_0\), \(\tilde{D}(E_F)\) is written as

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\]

Now, one can estimate relaxation time \(\tau_{ac}\) using the above expressions. If we choose the following material parameters, for example: acoustic deformation potential \(\Xi = 1.88\) eV,\(^{18}\) \(\rho = 2.33\) g/cm\(^3\),
\(v_s = 9000 \text{ m/s}, \ m^* = 0.15 \ m_0 \) (light hole mass), \(r_0 = 2.5 \text{ nm}, \ E_F = 10 \text{ meV}, \) and

\[\dot{D}(E_F) \equiv 2.0 \times 10^{45} / \text{J} \cdot \text{m}^3\] for our SiNW FET of 5 nm diameter, we estimate the acoustic scattering time \(\tau_{ac} \equiv 8.7 \times 10^{-12} \text{ s} \) at 300 K. Using \(\tau_{ac} \equiv 8.7 \times 10^{-12} \text{ s} \) and \(v_F (= \sqrt{2E_F / m^*}) \equiv 1.5 \times 10^5 \text{ m/s}, \) one can obtain the mean free path for carriers of light hole mass to be \(\ell_{ac} \equiv 1.3 \mu\text{m}. \) This is a direct result of narrow cross sectional dimensions of sub-5 nm and the square-root singular enhanced density of states at the 1D subband edges of the channel.

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